MOSFET

General Form

\[ M<name> \ (drain) \ node \ (gate) \ node \ (source) \ node \]
\[ + \ (bulk/substrate) \ node \ (model) \ name \]
\[ + \ L=\text{value} \ W=\text{value} \]
\[ + \ AD=\text{value} \ AS=\text{value} \]
\[ + \ PD=\text{value} \ PS=\text{value} \]
\[ + \ NRD=\text{value} \ NRS=\text{value} \]
\[ + \ NRG=\text{value} \ NB=\text{value} \]
\[ + \ M=\text{value} \]

Examples

\[ M1 \ 14 \ 2 \ 13 \ 0 \ P1 \ L=25u \ W=12u \]
\[ M13 \ 15 \ 3 \ 0 \ P2 \ L=25u \ W=12u \]
\[ M16 \ 17 \ 3 \ 0 \ P3 \ L=25u \ W=12u \]
\[ M28 \ 0 \ 2 \ 100 \ 100 \ W=2\text{mp} \ L=35u \ W=12u \]
\[ + \ AD=288p \ AS=288p \ PD=60u \ PS=60u \ NRD=14 \ NRS=24 \ NRG=10 \]

Model Forms

\[ \text{MODEL } M<name> \ \text{NMOS [(model parameters)]} \]
\[ \text{MODEL } M<name> \ \text{PMOS [(model parameters)]} \]

As shown in Figure 11, the MOSFET is modeled as an intrinsic MOSFET with ohmic resistances in series with the drain, source, gate, and bulk (substrate). There is also a shunt resistance (RDS) in parallel with the drain-source channel.

![MOSFET model](image)

Figure 11 MOSFET model.

PSpice provides four MOSFET device models, which differ in the formulation of the I-V characteristic. The LEVEL parameter selects between different models:
LEVEL=1 is the Shichman-Hodges model (see reference [1])
LEVEL=2 is a geometry-based, analytic model (see reference [2])
LEVEL=3 is a semi-empirical, short-channel model (see reference [2])
LEVEL=4 is the BSIM model (see reference [3])

L and W are the channel length and width, and are decreased to get the effective channel length and width. L and W can be specified in the device, model, or .OPTIONS statements. The value in the device statement supersedes the value in the model statement which supersedes the value in the .OPTIONS statement.

AD and AS are the drain and source diffusion areas. PD and PS are the drain and source diffusion perimeters. The drain-bulk and source-bulk saturation currents can be specified either by JS, which is multiplied by AD and AS, or by IS, which is an absolute value. The zero-bias depletion capacitances can be specified by Cj, which is multiplied by AD and AS, and by CJSW, which is multiplied by PD and PS. Or they can be set by CBD and CBS, which are absolute values.

NRD, NRS, NRG, and NRB are the relative resistivities of the drain, source, gate, and substrate in squares. These parasitic (ohmic) resistances can be specified either by RSH, which is multiplied by NRD, NRS, NRG, and NRB respectively or by RD, RS, RG, and RB, which are absolute values.

PD and PS default to 0, NRD and NRS default to 1, and NRG and NRB default to 0. Defaults for L, W, AD, and AS may be set in the .OPTIONS statement. If AD or AS defaults are not set, they also default to 0. If L or W defaults are not set, they default to 100u.

M is a device "multiplier" (default = 1), which simulates the effect of multiple devices in parallel. The effective width, overlap and junction capacitances, and junction currents of the MOSFET are multiplied by M. The parasitic resistance values (e.g. RD, RS) are divided by M. Note the third example showing a device twice the size of the second example.
Model Levels 1, 2, and 3

The DC characteristics of the first three model levels are defined by the parameters VTO, KP, LAMBDA, PHI, and GAMMA. These are computed by *P*Spice if process parameters (TOX, NSUB, ...) are given, but the user-specified values always override (Note: the default value for TOX is 0.1μ for model levels 2 and 3, but is unspecified for level 1 which "turns off" the use of process parameters). VTO is positive (negative) for enhancement mode and negative (positive) for depletion mode of N-channel (P-channel) devices.

<table>
<thead>
<tr>
<th>Model Parameters (see .MODEL statement)</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD</td>
<td>meter</td>
<td>0</td>
</tr>
<tr>
<td>WD</td>
<td>meter</td>
<td>0</td>
</tr>
<tr>
<td>VTO</td>
<td>volt</td>
<td>0</td>
</tr>
<tr>
<td>KP</td>
<td>amp/volt²</td>
<td>2E-5</td>
</tr>
<tr>
<td>LAMBDA</td>
<td>volt⁻¹</td>
<td>0</td>
</tr>
<tr>
<td>PHI</td>
<td>volt⁴/²</td>
<td>0</td>
</tr>
<tr>
<td>GAMMA</td>
<td>volt</td>
<td>calculated</td>
</tr>
<tr>
<td>TOX</td>
<td>meter</td>
<td>see above</td>
</tr>
<tr>
<td>TPG</td>
<td>+1</td>
<td></td>
</tr>
<tr>
<td>NSUB</td>
<td>1/cm²</td>
<td>none</td>
</tr>
<tr>
<td>NSS</td>
<td>1/cm²</td>
<td>none</td>
</tr>
<tr>
<td>NFS</td>
<td>1/cm²</td>
<td>0</td>
</tr>
<tr>
<td>XJ</td>
<td>meter</td>
<td>0</td>
</tr>
<tr>
<td>UO</td>
<td>cm²/volt·sec</td>
<td>600</td>
</tr>
<tr>
<td>UCRIT</td>
<td>volt/cm</td>
<td>1E4</td>
</tr>
<tr>
<td>UEXP</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>UTRA</td>
<td>(not used)</td>
<td></td>
</tr>
<tr>
<td>VMAX</td>
<td>meter/sec</td>
<td>0</td>
</tr>
<tr>
<td>NEFF</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>XQC</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>DELTA</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>THETA</td>
<td>volt⁻¹</td>
<td>0</td>
</tr>
<tr>
<td>ETA</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>KAPPA</td>
<td>saturation field factor</td>
<td>0.2</td>
</tr>
</tbody>
</table>


Model Level 4

The LEVEL = 4 (BSIM) model parameters are all values obtained from process characterization, and can be generated automatically. Reference [4] describes a means of generating a "process" file, which must then be converted into .MODEL statements for inclusion in a PSpice library or circuit file. (PSpice does not read process files.)

In the following list, parameters marked with a "*" in the L&W column also have corresponding parameters with a length and width dependency. For example, VFB is a basic parameter with units of volts, and LVFB and WVFB also exist and have units of volt · μ. The formula

\[ P_1 = P_0 + \frac{P_1}{L_e} + \frac{P_W}{W_e} \]

is used to evaluate the parameter for the actual device, where

\[ L_e = \text{effective length} = L - DL \]
\[ W_e = \text{effective width} = W - DW \]

Note that unlike the other models in PSpice, the BSIM model is designed for use with a process characterization system that provides all parameters: there are no defaults specified for the parameters, and leaving one out may cause problems.

<table>
<thead>
<tr>
<th>Model Parameters (see .MODEL statement)</th>
<th>Units</th>
<th>L&amp;W</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL</td>
<td>μ</td>
<td></td>
</tr>
<tr>
<td>DW</td>
<td>μ</td>
<td></td>
</tr>
<tr>
<td>TOX</td>
<td>μ</td>
<td></td>
</tr>
<tr>
<td>VFB</td>
<td>volt</td>
<td></td>
</tr>
<tr>
<td>PHI</td>
<td>volt</td>
<td></td>
</tr>
<tr>
<td>K1</td>
<td>volt</td>
<td></td>
</tr>
<tr>
<td>K2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ETA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X2E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X3E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MUS</td>
<td>cm²/volt · sec</td>
<td></td>
</tr>
<tr>
<td>U0</td>
<td>cm²/volt · sec</td>
<td></td>
</tr>
<tr>
<td>X2U0</td>
<td>cm²/volt · sec</td>
<td></td>
</tr>
<tr>
<td>U1</td>
<td>μ/volt</td>
<td></td>
</tr>
<tr>
<td>X2U1</td>
<td>μ/volt²</td>
<td></td>
</tr>
<tr>
<td>X3U1</td>
<td>μ/volt²</td>
<td></td>
</tr>
<tr>
<td>MUS</td>
<td>cm²/volt · sec</td>
<td></td>
</tr>
<tr>
<td>X2MS</td>
<td>cm²/volt · sec</td>
<td></td>
</tr>
<tr>
<td>X3MS</td>
<td>cm²/volt · sec</td>
<td></td>
</tr>
<tr>
<td>N0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEMP</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Measurement bias range
M MOSFET (cont.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>XPART</td>
<td>gate-oxide capacitance charge model flag</td>
<td></td>
</tr>
<tr>
<td>WDF</td>
<td>drain, source junction default width</td>
<td>meter</td>
</tr>
<tr>
<td>DELL</td>
<td>drain, source junction length reduction</td>
<td>meter</td>
</tr>
</tbody>
</table>

XPART = 0 selects a 40/60 drain/source charge partition in saturation, while XPART = 1 selects a 0/100 drain/source charge partition.
<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>XPART</td>
<td>gate-oxide capacitance charge model flag</td>
<td></td>
</tr>
<tr>
<td>WDF</td>
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<tr>
<td>DELL</td>
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<td>meter</td>
</tr>
</tbody>
</table>

XPART=0 selects a 40/60 drain/source charge partition in saturation, while XPART=1 selects a 0/100 drain/source charge partition.
For All Model Levels

The following list describes the parameters common to all model levels, which are primarily parasitic element values such as series resistance, overlap and junction capacitance, and so on.

Model Parameters (see .MODEL statement) Units Default
LEVEL model index 1
L channel length meter DEFL
W channel width meter DEFW
RD drain ohmic resistance ohm 0
RS source ohmic resistance ohm 0
RG gate ohmic resistance ohm 0
RB bulk ohmic resistance ohm 0
RDS drain-source shunt resistance ohm infinite
RSH drain, source diffusion sheet resistance ohm/square 0
IS bulk p-n saturation current amp 1E-14
JS bulk p-n saturation current/area amp/meter² 0
JSSW bulk p-n saturation sidewall current/length amp/meter 0
N bulk p-n emission coefficient 1
PB bulk p-n bottom potential volt 0.8
PBSW bulk p-n sidewall potential volt PB
CBD zero-bias bulk-drain p-n capacitance farad 0
CBS zero-bias bulk-source p-n capacitance farad 0
CJ bulk p-n zero-bias bottom capacitance/area farad/meter² 0
CJSW bulk p-n zero-bias sidewall capacitance/length farad/meter 0
MJ bulk p-n bottom grading coefficient 0.5
MJSW bulk p-n sidewall grading coefficient 0.33
FC bulk p-n forward-bias capacitance coefficient 0.5
TT bulk p-n transit time sec 0
CGSO gate-source overlap capacitance/channel width farad/meter 0
CGDO gate-drain overlap capacitance/channel width farad/meter 0
CGBP gate-bulk overlap capacitance/channel length farad/meter 0
KF flicker noise coefficient 0
AF flicker noise exponent 1

In the following equations:

\[ V_{gs} = \text{intrinsic gate-intrinsic source voltage} \]
\[ V_{gd} = \text{intrinsic gate-intrinsic drain voltage} \]
\[ V_{ds} = \text{intrinsic drain-intrinsic source voltage} \]
\[ V_{bs} = \text{intrinsic substrate-intrinsic source voltage} \]
\[ V_{bd} = \text{intrinsic substrate-intrinsic drain voltage} \]
\[ V_T = k \cdot T/q \text{ (thermal voltage)} \]
\[ k = \text{Boltzmann's constant} \]
\[ q = \text{electron charge} \]
\[ T^* = \text{analysis temperature (K)} \]
\[ T_{nom} = \text{nominal temperature (set with Tnom option)} \]

Other variables are from the model parameter list. These equations describe an n-channel MOSFET. For p-channel devices, reverse the signs of all voltages and currents. Positive current is current flowing into a terminal (for example, positive drain current flows from the drain through the channel to the source).
DC Currents

Note: positive current is current flowing into a terminal.

\[ I_g = \text{gate current} = 0 \]

\[ I_b = \text{bulk current} = I_{bs} + I_{bd} \]

\[ I_{bs} = \text{bulk-source leakage current} = I_{ss} \cdot (e^{\frac{V_{bs}}{V_{th}}} - 1) \]

\[ I_{bd} = \text{bulk-drain leakage current} = I_{ds} \cdot (e^{\frac{V_{bd}}{V_{th}}} - 1) \]

where if: \( JS = 0 \), or \( AS = 0 \), or \( AD = 0 \)

\[ I_{ss} = IS \]

\[ I_{ds} = IS \]

otherwise:

\[ I_{ss} = AS \cdot JS + PS \cdot JSSW \]

\[ I_{ds} = AD \cdot JS + PD \cdot JSSW \]

\[ I_d = \text{drain current} = I_{bd} - I_{drain} \]

\[ I_s = \text{source current} = I_{ds} + I_{drain} \]

Equations for \( I_{drain} \): LEVEL=1

For: \( V_{ds} \geq 0 \) (normal mode)

and: \( V_{gs} - V_{to} < 0 \) (cutoff region)

\[ I_{drain} = 0 \]

and: \( V_{ds} < V_{gs} - V_{to} \) (linear region)

\[ I_{drain} = (W/L) \cdot (K/2) \cdot (1 + \lambda \cdot V_{ds}) \cdot V_{ds} \cdot (2 \cdot (V_{gs} - V_{to}) \cdot V_{ds}) \]

and: \( 0 \leq V_{gs} - V_{to} \leq V_{ds} \) (saturation region)

\[ I_{drain} = (W/L) \cdot (K/2) \cdot (1 + \lambda \cdot V_{ds}) \cdot (V_{gs} - V_{to})^2 \]

where \( V_{to} = V_{TO} + \pi_{GAMMA} \cdot (V_{gs} - V_{to})^{1/2} \cdot (V_{gs} - V_{to})^{1/2} \)

For: \( V_{ds} < 0 \) (inverted mode)

Switch the source and drain in equations (above).

For LEVEL=2, or LEVEL=3, see reference [2] below for the equations describing \( I_{drain} \).
Capacitance

Note: all capacitances are between terminals of the intrinsic MOSFET. That is, to the inside of the ohmic drain and source resistances.

\[ C_{bs} = \text{bulk-source capacitance} = \text{area cap. + sidewall cap. + transit time cap.} \]

\[ C_{bd} = \text{bulk-drain capacitance} = \text{area cap. + sidewall cap. + transit time cap.} \]

For: \( CBS = 0 \) and \( CBD = 0 \)

\[ C_{bs} = AS \cdot CJ \cdot C_{bsj} + PS \cdot CJSW \cdot C_{bs} + TT \cdot G_{bs} \]

\[ C_{bd} = AD \cdot CJ \cdot C_{bdj} + PD \cdot CJSW \cdot C_{bd} + TT \cdot G_{ds} \]

otherwise

\[ C_{bs} = CBS \cdot C_{bsj} + PS \cdot CJSW \cdot C_{bs} + TT \cdot G_{bs} \]

\[ C_{bd} = CBD \cdot C_{bdj} + PD \cdot CJSW \cdot C_{bd} + TT \cdot G_{ds} \]

where

\[ G_{bs} = \text{DC bulk-source conductance} = \frac{dI_{bs}}{dV_{bs}} \]

\[ G_{bd} = \text{DC bulk-drain conductance} = \frac{dI_{bd}}{dV_{bd}} \]

For: \( V_{bs} \leq FC \cdot PB \)

\[ C_{bsj} = (1 - V_{bs}/PB)^{MJ} \]

\[ C_{bs} = (1 - V_{bs}/PBSW)^{MJSW} \]

For: \( V_{bs} > FC \cdot PB \)

\[ C_{bsj} = (1 - FC)^{MJSW} \cdot (1 - V_{bs}/PB) \cdot (1 - FC \cdot (1 + MJ) + MJ \cdot V_{bs}/PB) \]

\[ C_{bs} = (1 - FC)^{MJSW} \cdot (1 - FC \cdot (1 + MJ) + MJ \cdot V_{bs}/PBSW) \]

For: \( V_{bd} \leq FC \cdot PB \)

\[ C_{bdj} = (1 - V_{bd}/PB)^{MJ} \]

\[ C_{bd} = (1 - V_{bd}/PBSW)^{MJSW} \]

For: \( V_{bd} > FC \cdot PB \)

\[ C_{bdj} = (1 - FC)^{MJSW} \cdot (1 - FC \cdot (1 + MJ) + MJ \cdot V_{bd}/PB) \]

\[ C_{bd} = (1 - FC)^{MJSW} \cdot (1 - FC \cdot (1 + MJ) + MJ \cdot V_{bd}/PBSW) \]

Cgs = gate-source overlap capacitance = CGSO \cdot W

Cgd = gate-drain overlap capacitance = CGDO \cdot W

Cgb = gate-bulk overlap capacitance = CGBO \cdot L

See reference [2] for the equations describing the capacitances due to the channel charge.
Temperature Effects

\[ IS(T) = IS \cdot e^{(Eg(T)_{nom}) \cdot \frac{T}{T_{nom}} \cdot \frac{Eg(T)}{Vt}} \]

\[ JS(T) = JS \cdot e^{(Eg(T)_{nom}) \cdot \frac{T}{T_{nom}} \cdot \frac{Eg(T)}{Vt}} \]

\[ JSSW(T) = JSSW \cdot e^{(Eg(T)_{nom}) \cdot \frac{T}{T_{nom}} \cdot \frac{Eg(T)}{Vt}} \]

\[ PB(T) = PB \cdot \frac{T}{T_{nom}} \cdot 3 \cdot Vt \cdot ln(T/T_{nom}) - Eg(T)_{nom} \cdot T \cdot T_{nom} + Eg(T) \]

\[ PBSW(T) = PBSW \cdot \frac{T}{T_{nom}} \cdot 3 \cdot Vt \cdot ln(T/T_{nom}) - Eg(T)_{nom} \cdot T \cdot T_{nom} + Eg(T) \]

where \( Eg(T) = \) silicon bandgap energy = 1.16 - 0.000702 \( \cdot T^2 \)/\( T+1108 \)

\[ CBD(T) = CBD \cdot (1+MJ \cdot 0.0004 \cdot (T-T_{nom}) + (1-PB(T)/PB)) \]

\[ CBS(T) = CBS \cdot (1+MJ \cdot 0.0004 \cdot (T-T_{nom}) + (1-PB(T)/PB)) \]

\[ CJ(T) = CJ \cdot (1+MJ \cdot 0.0004 \cdot (T-T_{nom}) + (1-PB(T)/PB)) \]

\[ CJSW(T) = CJSW \cdot (1+MJ_{SW} \cdot 0.0004 \cdot (T-T_{nom}) + (1-PB(T)/PB)) \]

\[ KP(T) = KP \cdot (T/T_{nom})^{-3/2} \]

\[ UO(T) = UO \cdot (T/T_{nom})^{-3/2} \]

The ohmic (parasitic) resistances have no temperature dependence.

Noise

Noise is calculated assuming a 1 Hertz bandwidth, with the following spectral power densities (per unit bandwidth):

- the parasitic resistances (Rd, Rg, Rs and Rb) generate thermal noise ...
  \[ Id^2 = 4 \cdot k \cdot T / Rd \]
  \[ Ig^2 = 4 \cdot k \cdot T / Rg \]
  \[ Is^2 = 4 \cdot k \cdot T / Rs \]
  \[ Ib^2 = 4 \cdot k \cdot T / Rb \]

- the intrinsic MOSFET generates shot and flicker noise ...
  \[ Idrain^2 = 4 \cdot k \cdot T \cdot gm \cdot 2/3 + KF \cdot Idrain^{AF} / (FREQUENCY \cdot Kchan) \]
  where
    \[ gm = dIdrain/dVgs \] (at the DC bias point)
    \[ Kchan = \text{(effective length)}^2 \cdot \text{(permittivity of SiO}_2) / \text{TOX} \]
References

For a more complete description of the MOSFET models, see:


References [2] and [4] are available for $10.00 (each) by sending a check payable to The Regents of the University of California to this address:

Cindy Manly
EECS/ERL Industrial Support Office
497 Cory Hall
University of California
Berkeley, CA 94720